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## 1 Scope and Purpose

This specification defines the minimum acceptable requirements applicable to the fabrication of printed boards for Benchmark. Compliance to this specification is mandatory unless Benchmark provides a written waiver. The purpose of this specification is to address manufacturing requirements for Benchmark and should be used as a supplement to the specifications called out on the supplied fabrication drawings.

This specification applies to all printed boards fabricated for Benchmark, when specified in the Purchase Order or in a Supplier Agreement. This specification may be shared between customers, fabricators and Benchmark site in accordance with an NDA and/or MSA. This document is intended to be used by Benchmark SDE, SQE, incoming inspectors and fabricators.

## 2 References



Ref Number	Title
BE-46013	ENIG Black Pad Analysis Protocol
IPC-1602	Standard for Printed Board Handling and Storage
IPC-1752	Materials Declaration Management
IPC-4101	Specifications for Base Materials for Rigid and Multilayer Printed Boards
IPC-4202	Flexible Base Dielectrics for Use in Flexible Printed
IPC-4203	Cover and Bonding Material for Flexible Printed Circuitry
IPC-4204	Flexible Metal-Clad Dielectrics for Use in Fabrication of Flexible Printed Boards
IPC-4552	Performance Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Boards
IPC-4553	Specification for Immersion Silver Plating for Printed Boards
IPC-4554	Specification for Immersion Tin Plating for Printed Boards
IPC-4556	Specification for Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG) Plating for Printed Boards
IPC-4761	Design Guide for Protection of Printed Board Via Structures
IPC-4781	Qualification and Performance of Permanent, Semi-Permanent and Temporary Legend and/or Marking Inks
IPC-6012	Qualification and Performance Specification for Rigid Printed Boards.
IPC-6013	Qualification and Performance Specification for Flexible Printed Boards.
IPC-9252	Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards
IPC-7721	Repair and Modification of Printed Boards and Electronic Assemblies
IPC-A-600	Acceptability of Printed Boards
IPC-TM-650	Test Methods Manual
IPC-SM-840	Qualification and Performance of Permanent Solder Mask and Flexible Cover Materials
J-STD-003	Solderability Tests for Printed Boards
J-STD-020	Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices
J-STD-609	Marking and Labeling of Components, PCBs and PCBAs to Identify Lead (Pb), Pb-Free and Other Attributes
UL 796	UL Recognized Component Index

### 3 Definitions and Abbreviations

Definitions and abbreviations can also be found in Global Record, Benchmark Glossary

Term/Abbreviation	Definition
<b>AABUS</b>	As Agreed Between User and Supplier
<b>AOI</b>	Automated Optical Inspection: Camera-based method to perform visual inspection.
<b>Base Material</b>	The laminate and/or prepregs used to fabricate the printed board. A prepreg is a sheet of material that has been impregnated with a resin cured to an intermediate stage, i.e., B-staged resin.
<b>CAF</b>	Conductive Anodic Filamentation or Conductive Anodic Filament growth: An electrical short which occurs in a printed board when a conductive filament forms in the laminate (dielectric) material between two adjacent conductors under an electrical bias. CAF should be taken under consideration if hole-to-hole spacing is 0.025" (0.64 mm) or less.
<b>C of C</b>	Certificate of Compliance: A supplier's declaration that a batch lot of printed boards was verified, prior to shipment, to satisfy all fabrication specifications.
<b>DTP</b>	Diameter of True Position: A circle of a given diameter centered on a specified or theoretical location. Common method for determining location tolerances for printed board features and holes.
<b>Dry Packaging</b>	That consists of desiccant material and a Humidity Indicator Card (HIC) sealed with the printed boards inside a Moisture Barrier Bag (MBB).
<b>Element Symbols</b>	Bromine (Br)    Copper (Cu)    Gold (Au)    Lead (Pb) Nickel (Ni)    Palladium (Pd)    Phosphorus (P)    Silver (Ag) Tin (Sn)
<b>ENIG</b>	Electroless Nickel/Immersion Gold Plating: Printed board surface finish
<b>ENEPIG</b>	Electroless Nickel/Electroless Palladium/Immersion Gold: finish
<b>FAIR</b>	First Article Inspection Report: A report provided by supplier.
<b>FHS</b>	Finished Hole Size
<b>First Pass Yield</b>	The percentage of items that were accepted through an inspection or testing operation on the first pass (prior to adjustment, touch-up, rework, etc.).
<b>Flashing</b>	Material added to an assembly array for machine transfer and handling during assembly. Also referred to as breakaway

	features, these are removed at a depanelization step during production.
<b>HAL or HASL</b>	Hot Air Leveling or Hot Air Solder Level: A solder coating process in which a panel of printed boards are submerged in molten solder. An air knife is used to remove excess solder and planarize the surface.
<b>Halogen-Free Base Material</b>	Printed board resins plus reinforcement matrix that contain maximum total halogens of 1500 ppm with less than 900 ppm bromine and less than 900 ppm chlorine. The marking "HF" may be noted on the printed board.
<b>HIC</b>	Humidity Indicator Card: A card on which a moisture-sensitive chemical is applied such that it will make a significant, perceptible change in color (hue), typically from blue (dry) to pink (wet) when the indicated relative humidity is exceeded. The HIC is packed inside the moisture-barrier bag (MBB), along with a desiccant, to aid in determining the level of moisture to which the moisture-sensitive devices or printed boards have been subjected.
<b>IAG</b>	Immersion Silver: Printed board surface finish.
<b>ISn</b>	Immersion Tin: Printed board surface finish.
<b>Impedance</b>	A critical electrical property of transmission lines and high-frequency circuits. Affected by conductor cross-section, surrounding dielectric (insulating) material, and distance to adjacent conductor(s) or plane(s).
<b>Ionic Cleanliness</b>	The degree of surface freedom from contamination as measured by the weight of ionic matter per square unit of surface area. It is a figure of merit used to evaluate the effectiveness of a cleaning procedure.
<b>Laminate Characteristics</b>	<p>These are used for selecting the appropriate laminate materials</p> <p><b>CTE Coefficient of Thermal Expansion</b> - For glass reinforced laminates the XY CTE is typically 16-18 PPM below its <math>T_g</math> temperature. The Z axis is usually 55-60 PPM below its <math>T_g</math> temperature. CTE increases dramatically above the laminates glass transition temperature.</p> <p><b>Td Thermal Decomposition Temperature</b> - Measured as the mass loss versus temperature of a laminate. The temperature required for the laminate sample to lose 5% of its mass.</p> <p><b>Tg Glass Transition Temperature</b> - The temperature where the printed board resin system transitions from a rigid solid to a semi-solid (softens). Below the <math>T_g</math> the CTE is relatively low and</p>

	<p>linear. Above the <math>T_g</math> the expansion rate increases dramatically. <math>T_g</math> is measured by Thermal Mechanical Analysis (TMA).</p> <p><b>Time to Delamination T260/T288 (TMA)</b> - The test time that a laminate sample can withstand before a catastrophic failure occurs resulting in delamination.</p>				
<b>Pb-Free Symbol</b>	<p>Per J-STD-609 this symbol may be used in addition to, or instead of the phrase "Pb-Free", or "lead free."</p> 				
<b>Micro Inch (<math>\mu\text{in}</math>)</b>	millionths of an inch				
<b>Micron (<math>\mu\text{m}</math>)</b>	millionths of a meter ( $1 \mu\text{m} \approx 39.4 \mu\text{in}$ )				
<b>Minimum Conductor Spacing</b>	The distance between the two closest points of two adjacent coplanar conductors, measured between the bases of two etched conductors.				
<b>MBB</b>	Moisture Barrier Bag: A bag designed to restrict the transmission of water vapor and used to pack moisture sensitive devices. An MBB is made of material with a low WVTR.				
<b>Non-Ionic</b>	A substance that does not ionize (lose electrons) in water. Non-ionic residues are insulators, and can cause intermittent or inoperative electrical performance, especially when they appear on the surfaces of connector contacts.				
<b>NPTH</b>	Non-plated Through Hole: Is a hole through the printed board that is not metal-plated. It typically requires a minimum clearance from adjacent conductors on external and internal layers.				
<b>OSP</b>	Organic Solderability Preservative: a surface coating applied to printed boards.				
<b>Printed Board Surface Finish Categories</b>	<p>Per J-STD-609 the categories b0 thru b9 are used to describe the predominant surface finish on the bare board (prior to assembly).</p>  <p>These are example marks indicating Surface Finish Category 4 with the optional circle, ellipse, underline or parentheses. Note the letter "b" would be replaced with letter "e" for identifying Material Category Symbols for component terminals.</p> <table border="1"> <thead> <tr> <th>Category</th> <th>Printed Board Surface Finish Description</th> </tr> </thead> <tbody> <tr> <td>b0</td> <td>Contains lead. Typically, tin/lead (SnPb) like HASL</td> </tr> </tbody> </table>	Category	Printed Board Surface Finish Description	b0	Contains lead. Typically, tin/lead (SnPb) like HASL
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<b>PTH</b>	Plated Through Hole: Is a metal-plated hole that connects internal and/or external conductors on a printed board. Connectors and other through-hole components may be soldered to the plated-through holes of a printed board.														
<b>RoHS</b>	<p>The part(s) referenced in the certificate of compliance shall meet the requirements of the RoHS Directive 2011/65/EC, Amended with Directive (EU) 2015/863. This may include printed boards, cables, hardware and cabinets, but does not include material used to ship the product.</p> <p><b>RoHS</b> (Directive 2002/95/EC) stands for Restriction of Hazardous Substances. It originated in the European Union in 2002 and restricts the use of six hazardous materials found in electrical and electronic products. All applicable products in the EU market since July 1<sup>st</sup>, 2006, must pass RoHS compliance.</p> <p><b>RoHS 2</b> (Directive 2011/65/EU) was published in 2011 by the EU. It includes a CE-marking directive, added Categories 8 and 9, and has additional compliance recordkeeping requirements.</p> <p><b>RoHS 3</b> (Directive 2015/863) adds four additional restricted substances (phthalates) to the list of six.</p> <p>The first six substances apply to the original RoHS while <b>RoHS 3</b> adds four additional restricted substances which took effect July 22, 2019.</p> <table border="1"> <thead> <tr> <th>Banned Substance</th> <th>Limit</th> </tr> </thead> <tbody> <tr> <td>Cadmium (Cd)</td> <td>&lt; 100 ppm</td> </tr> <tr> <td>Lead (Pb)</td> <td>&lt; 1000 ppm</td> </tr> <tr> <td>Mercury (Hg)</td> <td>&lt; 1000 ppm</td> </tr> <tr> <td>Hexavalent Chromium (Cr VI)</td> <td>&lt; 1000 ppm</td> </tr> <tr> <td>Polybrominated Biphenyls (PBB)</td> <td>&lt; 1000 ppm</td> </tr> <tr> <td>Polybrominated Diphenyl Ethers (PBDE)</td> <td>&lt; 1000 ppm</td> </tr> </tbody> </table>	Banned Substance	Limit	Cadmium (Cd)	< 100 ppm	Lead (Pb)	< 1000 ppm	Mercury (Hg)	< 1000 ppm	Hexavalent Chromium (Cr VI)	< 1000 ppm	Polybrominated Biphenyls (PBB)	< 1000 ppm	Polybrominated Diphenyl Ethers (PBDE)	< 1000 ppm
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		<b>Bis(2-Ethylhexyl) Phthalate (DEHP)</b>	< 1000 ppm
		<b>Benzyl Butyl Phthalate (BBP)</b>	< 1000 ppm
		<b>Dibutyl Phthalate (DBP)</b>	< 1000 ppm
		<b>Diisobutyl Phthalate (DIBP)</b>	< 1000 ppm
<b>SMOBC</b>	Solder Mask Over Bare Copper: A printed board technology where bare copper conductors are protected with a mask, leaving only component lands exposed for plating, and final board finish application.		
<b>Solderability</b>	One of the two primary functions of a board finish is to provide a solderable surface finish capable of providing a coating durability rate of B, per the IPC-J-STD-003. Coating Durability B is defined as: Intended for boards likely to experience multiple soldering processes and/or other process steps using SnPb or Pb-Free assembly profiles. The solderability requirement is for all finished SMT features tested to wet with solder covering at least 95% of each feature. All tested PTHs can achieve fully wetted walls of the hole, and no non-wetting or exposed base material occurs on any tested PTH.		
<b>Sub-Panel</b>	An arrangement of one or more printed boards with the same part number and revision level, within or connected to a framework, which will be separated after delivery to Benchmark. Can include multiple boards, rails, stiffeners, or filler areas; also known as a Palletized Array.		
<b>SDE</b>	Supplier Development Engineer: An individual responsible for driving improvement activities with our suppliers.		
<b>SQE</b>	Supplier Quality Engineer: individual responsible for setting requirements for vendors, measuring compliance to these requirements.		
<b>SCA</b>	Supply Chain Analyst: an individual responsible for providing purchase order to printed board fabricator.		
<b>Sigma</b>	The standard deviation(s) measured from the mean		
<b>Thieving</b>	A pattern of copper features added to one or both outer layers of a printed board to balance and equalize plating currents across the area of a panel. Similar patterns can also be used as filler on inner layers.		
<b>Via</b>	A plated-through hole that is used to make connections among different layers of a printed board.  <b>Microvia</b> - A Microvia is any Via, Blind, Buried, or Plated-Through-Hole that is 6 mils or less in diameter. It can be formed by Laser drill, Mechanical Drill, or by other processes.		

	<p><b>Stacked Microvia</b> - A process where adjacent layer microvias are placed one on top the other (stacked) to increase the interconnection density of a printed board design.</p> <p><b>Blind Via</b> - Does not pass through the entire board and has access to only one external layer (incomplete penetration).</p> <p><b>Buried Via</b> - Provides connector within inner layers and does not access either external layer (non-surfacing).</p> <p><b>Plated Through Hole Via</b> - Passes through the entire thickness of the printed board and has access to both external layers and internal layers as required.</p>
<b>VIPPO</b>	Via In Pad Plated Over: The name is not mentioned in IPC-6012, but is often referenced in the printed board fabrication industry in place of copper cap plating of filled holes as defined in section 3.6.2.11.2.
<b>WVTR</b>	Water Vapor Transmission Rate: A measure of the permeability of plastic film or metallized plastic film material to moisture, an important rating for moisture barrier bags (MBBs).
<b>X-Out</b>	A method of identifying one or more printed boards within a sub-panel as unusable (an electrical test failure or inspection failure).
<b>XRF</b>	X-Ray Fluorescence: a non-destructive method of measuring coating thickness.

## 4 Requirements

### 4.1 Order of Precedence

- a) Purchase Order
- b) Part Specific Design Package (ODB++ and/or Gerber)
- c) Part Specific Fabrication Drawing including panel drawing as required
- d) OEM Customer's Specification if referenced in PO or Fabrication Drawing
- e) Compliance to this document (BE-46003)
- f) Printed boards shall conform to the requirements of IPC-6012 Class 2 and acceptability of companion document IPC-A-600 Class 2. (IPC-6013 Class 2 would apply for flex circuits).

### 4.2 Compliance Verification

Printed board suppliers need to follow requirements of this document. Compliance verification to this document may include:

- supplier audit,



- incoming inspection of bare boards, and
- Benchmark review of supplier C of C through certificate verification. This is usually accomplished by repeating select measurements while following IPC-TM-650 methods. Benchmark groups acting as SCA, SDE, SQE, and Purchasing agents are responsible for providing this document to printed board suppliers.

### 4.3 Supplier Responsibilities

- The supplier is responsible for correct photo tool and fabrication database generation from the supplied design package without plot approvals from Benchmark.
- It is the supplier's responsibility to ensure that the revisions on the Benchmark purchase order match the revisions on the Benchmark part specific printed board fabrication drawings and design package.
- It is the supplier's responsibility to run a complete Design Rules check on the supplied electronic data to identify potential violations, and to compare this data to the supplied part specific drawings to review for potential discrepancies. If the artwork is modified the supplier shall compare the changes to the source data to make sure that the design has not been violated. The supplier shall communicate any discrepancies or requests for deviation to Benchmark, in writing, prior to fabricating the boards.
- Problems and deviations that are discovered during the supplier's review or setup, and fabrication process will be handled by placing the parts ON Hold until the question is resolved or by a Waiver Request and Approval before the finished parts are shipped.
- Once a part has been fabricated and accepted by Benchmark it is considered qualified using a particular series of process steps that does not change. This does not apply to bath change-outs and corrections that are part of routine operations. If the process is changed to a different chemical makeup or a different vendor, the manufacturing process may need to be requalified at Benchmark's discretion before more boards are accepted.
- No portion of the manufacturing, testing or inspecting of any product for Benchmark may be sub-contracted to another supplier, without prior written authorization. This requirement does not include sub-contracted suppliers that perform tasks within the facility of the Benchmark supplier. (i.e., An in-house store process)
- The Supplier is responsible for ensuring that adequate process controls are in place to provide quality product to Benchmark. The supplier must make this data available to Benchmark upon written request.

### 4.4 X-Outs

- No X-outs are allowed on panelized boards unless defined on Customer / Benchmark array drawing without prior written authorization from Purchasing / SCA and SDE.
- When authorized, a panel drawing note or customer specification shall indicate the number of X-outs and the marking requirements. The scrap boards shall have an "X" marked on both sides with permanent black ink, and a corresponding Image Reject Mark per X-out board should also be blacked out when defined. There must be no cut-outs in X-out boards. Sub-panels containing X-outs must be packaged separately and labeled.

#### 4.5 Shelf Life

- Benchmark will not accept boards with less than 50% of the expected shelf life remaining as determined by board finish, unless pre-approved by SDE / SQE.
- 1 year shelf life: ENIG, ENEPIG, Flash Gold, Immersion Silver, SN100CL (LF HASL), and PB HASL
- 6-month shelf life: OSP and Immersion Tin
- If OSP application date is different than the date code marking, then call it out separately on the C of C.
- If printed board supplier is using a surface finish chemistry with different stated manufacturer shelf life, then that information should be documented with deliverables reporting, and/or labeled on the bags.
- In cases where removing the old finish and applying a new finish is being considered:
  - Approval prior to stripping finish is required,
  - proper fabrication and storage requirements have been followed, and
  - solderability test coupons and results shall be included with printed boards.

### 5 Acceptability Requirements

Unless otherwise specified in this General Specification or in a Superseding Document, all printed boards and sub-panels must satisfy the requirements listed as “Class 2” in the following documents (current revision):

- IPC-A-600: Acceptability of Printed Boards
- IPC-6012: Qualification and Performance Specification for Rigid Printed Boards.
- IPC-6013: Qualification and Performance Specification for Flexible Printed Boards.

The following Sections describe additions to or exceptions from those requirements.

#### 5.1 Added Features

When approved by the customer, copper features (e.g., thieving) added within the board outline shall have a non-interconnected pattern of 0.050” features on 0.100” centers. Thieving features may not be closer than 0.050” to any defined copper feature, or board edge. All copper patterns added to outer layers by the fabricator must be fully covered by solder mask. Solder mask must extend a minimum of .025” past the edge of any copper patterns added by the fabricator.

#### 5.2 Base Material

All base materials (core laminates and prepregs) shall have a UL flammability rating of 94V-0, as determined by UL Standard 796, current revision.

#### 5.3 Conductor Definition / Etching

- Surface Mount pad exception: Non solder mask defined lands with a diameter, or both X and Y dimensions are less than 0.010” shall be held to within +0.0015”/-0.0011” of the electronically defined nominal pad dimension.

- External pad breakout is unacceptable. The minimum conductor to land junction interface shall never be less than 0.002”.
- Layer to Layer registration between all layers shall not exceed a positional tolerance of  $\pm 0.005$ ”.

#### 5.4 Laminate Construction

- Weave exposure between conductors is not acceptable for Class 2 (same as Class 3).
- Subsurface Imperfections and Foreign Inclusions: Subsurface imperfections shall be treated as Foreign Inclusions when determining acceptability per IPC 600 Class 2 (same as Class 3), with the following restrictions:
- Translucent imperfections cannot bridge conductors, and when located between conductors, the imperfections cannot reduce spacing more than 50 %.
- The imperfection cannot propagate as the result of testing or processing.

#### 5.5 Bow and Twist

- Bow and Twist shall be measured using IPC-TM-650 number 2.4.22.
- Bow and twist shall be 70 microns per centimeter (7 mils per inch) maximum. The maximum bow and twist shall not exceed 1.8 mm (70 mils) across the entire printed board regardless of width or length. The bow and twist in areas of array packages like BGAs and CGAs shall not exceed 30 microns per centimeter (3 mils per inch).

#### 5.6 Copper Plating

- Electroless copper shall be used only as a preliminary process to provide a conductive surface for Electro-plated copper. Direct metallization and full build Electroless copper methods are not acceptable without prior written approval from Benchmark.
- Copper plating voids shall meet IPC-6012 Class 3.
- Methods used to monitor the copper plating must include micro-sections of the smallest plated hole size and at least one component hole for the specific part number being built (minimum of 3 holes) from an area of the board having the lowest plating current density. See section 11 Micro-sectioning.
- The supplier is required to keep the actual micro-sections for at least one year and be able to provide the micro-section upon request from Benchmark.
- Printed board circuitry must conform to IPC - 6012 Class 2 except the minimum average copper thickness in all plated through holes, blind vias, and buried vias shall be 25.4 microns (1.0 mils) with the minimum measurement of at least 20.3 microns (0.8 mils).
- The minimum internal annular ring must be 25.4 microns (1 mil) at land / conductor junction, and tangency elsewhere.
- The minimum external annular ring must be 50.8 microns (2 mils) at land / conductor junction, and 25.4 microns (1 mil) elsewhere.
- Wicking allowance of copper in any plated through hole must not exceed IPC A-600 Class 3; 80 microns (3.15 mils).

## 5.7 Flex and Rigid Flex

Products that are constructed using flexible metal-clad dielectrics shall be compliant to IPC-4204. For example the material supplier of copper clad polyimide dielectric with acrylic adhesive must assure it has been manufactured, tested and certified in accordance to the IPC-4204/1 specification.

The use of covers, adhesives and bonding films shall be compliant to the IPC-4203. For example the material supplier of acrylic adhesive on one or both sides of polyimide dielectric must assure it has been manufactured, tested and certified in accordance to the IPC-4203/1 specification.

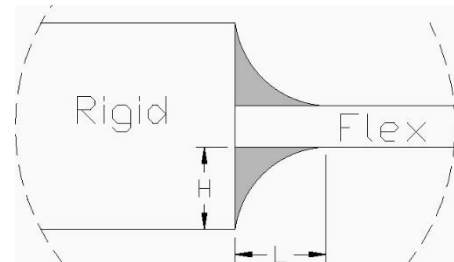
### 5.7.1 Acrylic Adhesive Cut-Back

Rigid Flex constructions use coverlay material to insulate the circuitry on the flexible layers and is typically bonded with acrylic adhesives. The acrylic adhesive shall NOT extend more than .050" into the rigid portion of the design to avoid reliability issues in the plated through-hole areas. "Cut-back" refers to cutting back the acrylic adhesive, so it is not extended into the rigid portion of the stack-up

### 5.7.2 Adhesive Fillets or Strain Relief at Rigid Flex Transition

Rigid-flex transition areas shall have an adhesive fillet or strain relief material applied. The rigid portion can be a printed board or a partial stiffener. The adhesive fillets can be flexible epoxies or acrylics. The adhesive fillets are to reduce stress at the rigid-flex transition when formed. The adhesive fillet target condition:

- Fillet shall extend up vertical surface  $\geq 0.7H$ , or 30 mils whichever is less.
- $L = 2H \pm H$
- Strain relief material shall not flood onto rigid board surface.
- Strain relief material shall not encroach the designated bend radius area of flex.



**Figure 5-1: Adhesive Fillet at Rigid Flex Transition**

## 5.8 Solder Mask

### 5.8.1 General

- Solder mask shall be in accordance with IPC-SM-840 type photoimageable (LPI) class T/FT (Telecommunications) for Class 2 product, and class H/FH (High Reliability/ Military) for Class 3 product.
- Solder mask over bare copper shall be used.
- The color shall be green unless stated otherwise.
- There shall be no missing solder mask on or between conductors.
- The solder mask type shall provide a matte or satin finish. Glossy or Semi-gloss finishes are not allowed.

### 5.8.2 Solder Mask LDI and LPI

- Non-Solder Mask Defined pads have design data that includes a solder mask clearance typically 2 to 3 mils per side larger than the associated copper pad. Solder mask shall not encroach onto these copper lands.
- When solder mask apertures are 1:1 with their associated copper pads the fabricator may add clearance (swell) to prevent solder mask from encroaching onto these copper lands.
- Solder mask defined pads have solder mask apertures smaller than their associated copper pads. The fabricator in conjunction with the fabrication notes allowable shall target the nominal size aperture per the design data with a maximum tolerance of  $\pm 2$  mils for LPI.
- Laser direct imaging of solder mask may be used on high density designs when solder mask tolerances need to be held to within  $\pm 1.3$  mils of the design data.

### 5.9 Via Treatment

The printed board design package contains graphical layers for solder mask and/or cover layers. The intentional covering of vias may be represented by not providing openings on the corresponding solder mask and/or cover layers.

Encroached vias may be represented by providing openings smaller than the copper via pads, but larger than the intended FHS on the corresponding solder mask and/or cover layers. Often these solder mask openings are 6-8mils larger than the FHS.

Vias that are represented by an opening that is 1:1, or slightly larger than the corresponding copper via pad are intended to be clear of solder mask or cover layer material.

#### 5.9.1 Via Plugging

IPC4761 Table 5-1 identifies via protection types. Via plugging and via encroachment is often associated with BGAs. Thermal pads for Dpaks and bottom terminal components like: QFNs, SONs, and LGAs are also popular applications.

- Single sided via protection IPC-4761 (Types I-A, II-A and III-A) should not be used with bare copper hole walls. It is recommended that OSP receive a complete fill or plugged from both sides.
- Plugging vias from both sides of the printed board by the fabricator shall utilize a process that addresses the concerns of air entrapment / outgassing events by using a secondary LPI or dry film tenting instead of a single flooding of the printed board surface with solder mask. This applies to IPC-4761 Type III-B and Type IV-B vias.
- Bump height of the plug/mask material shall not exceed 0.051 mm (2mils) greater than the copper via pad, or adjacent solderable land.
- Test point vias identified in Design Package must not be plugged from the probed side of the printed board.

If the part specific design package does not address the via treatment intent in the CAD layers or fabrication drawing notes, please notify Benchmark. The data can then be reviewed for proper disposition.

### 5.9.2 Filled and Capped Vias

**VIPPO (Via In Pad Plated Over):** Plated through hole vias shall be filled (call out sizes in FHS table) with a non-conductive polymer. Filled vias shall be planarized and plated over with copper on both sides of the printed board. The copper cap plating of filled holes must meet the copper cap, via depression (Dimple) and protrusion (Bump) requirements of IPC-6012E Table 3-11, Class 3.

**Copper Filled Vias:** When copper filled vias are specified (call out sizes in FHS table) through vias shall be plated shut with copper, subject to the acceptability requirements of IPC-6012E Section 3.6.2.11.3 and Figure 3-32. These requirements may be applied to Through, Blind, Buried and Microvia structures.

**Special requirement:** When 100% of the specified holes are to be sealed and air leakage shall be considered cause for printed board rejection an IPC-4761 Type VII (VIPPO) via shall be used.

### 5.10 Surface Finishes

Printed boards delivered to Benchmark shall have one of the following final finishes.

- Electroless nickel-immersion gold (ENIG)
- Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG)
- Electroplated nickel-gold
- Immersion Tin
- Immersion Silver
- Organic solderability preservative (OSP)
- HAL (Pb-free)
- Hot Air Solder Leveling (HASL and Plated and Reflowed SnPb)

Any other finish requires prior approval, via ECN, from Benchmark. During the processing of the subject printed boards the supplier shall certify that all processing parameters in the surface finish process flow remained within the chemistry supplier's published recommended limits.

#### 5.10.1 Electroless Nickel-Immersion Gold (ENIG)

- ENIG finish shall adhere to IPC-4552.
- ENIG plating finish to be deposited after solder mask.
- Full body ENIG processing is not allowed.
- XRF results shall be reported in Certificate of Compliance under Section 13 Supplier Deliverables for the Immersion Gold and Electroless nickel thicknesses.

- Shelf life of the finish is 1 year from date of manufacture and shall be packaged in moisture sensitive packaging per IPC-1602.

BE-46013 ENIG Black Pad Analysis Protocol to be provided in instances when ENIG finish performance concerns require failure analysis.

#### **5.10.2 Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG)**

- ENEPIG finish shall adhere to IPC-4556 for soldering purposes. The packaging requirements for ENIG can be used.
- If the ENEPIG finish must enable Micro Electronics (wire bonding, stud bump bonding, etc.), then palladium and gold thicknesses parameters may need to be optimized outside of current IPC-4556 parameters.
- Board surfaces should be protected from scratches and mechanical damage that may occur during shipping and handling, using interleaf papers that are pH neutral and sulfur free (e.g., Silver Saver® paper) shall be used.
- ENEPIG plating finish to be deposited after solder mask.
- XRF results shall be reported in Certificate of Compliance under Section 13 Supplier Deliverables for the Immersion Gold and Electroless nickel thicknesses.
- Shelf life of the finish is 1 year from date of manufacture and shall be packaged in moisture sensitive packaging per IPC-1602.

#### **5.10.3 Immersion Silver (IAg)**

- Immersion Silver finish shall adhere to IPC-4553.
- XRF results shall be reported in Certificate of Compliance under Section 13 Supplier Deliverables for the IAg thickness.
- Shelf life of the finish is 1 year from date of manufacture and shall be packaged in moisture sensitive packaging per IPC-1602.

#### **5.10.4 Immersion Tin (ISn)**

- Immersion Tin finish shall adhere to IPC-4554.
- No evidence of Tin Whiskers after 14 weeks of storage.
- XRF results shall be reported in Certificate of Compliance under Section 13 Supplier Deliverables for the ISn thickness.
- Shelf life of the finish is 6 months from date of manufacture and shall be packaged in moisture sensitive packaging per IPC-1602.

#### **5.10.5 Organic Solderability Preservative (OSP)**

- Regardless of the chemical used, the responsibility for a solderable surface will be the suppliers. The OSP surface treatment must provide excellent solderability and protection of the bare copper for at least 6 simulated reflow profiles of 260° C peak temperature with ~100 seconds above the liquidus ( $\geq 217^\circ\text{C}$ ) temperature.
- OSP must not deposit or stain gold surfaces in mixed metal designs.
- Shelf life of the finish is 6 months from date of manufacture and shall be packaged in moisture sensitive packaging per IPC-1602. Packaging materials shall be sulfur free.

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**5.10.6 HASL (Tin-Lead) Non-RoHS**

- Bulk solder used for SnPb solder coating must be at 60%-70% tin and must comply with J-STD-006. Fused tin-lead plating must have 50%-70% tin content.
- All printed boards must satisfy the requirements of J-STD-003, without pretreatment, for at least 12 months after delivery to Benchmark. Exposed copper on any conductor surface is not permitted. Solder coatings must have a smooth, homogeneous appearance on all coated surfaces, with no evidence of non-wetting or de-wetting.
- Solder finish thickness is to be measured where applicable by XRF at the geometric center of the pads. If there is a visibly thick area of the deposit, the thickness shall be measured at the thickest part of the solder. Pads selected for measurement must include: pads of the finest pitch (one pad in both the X and Y direction must be measured), pads of the next finest pitch, 50 mil pitch pads, and a capacitor/resistor pad. Measurements must be taken on both sides of the board. The solder coating shall have an average solder thickness between 100 micro-inches and 1000 micro-inches with no points above 1500 micro-inches. Isolated areas may be as low as 50 micro-inches if they maintain a solderable surface. The pad must be visually bright and smooth when viewed at 3X.
- XRF results shall be reported in Certificate of Compliance under Section 13 Supplier Deliverables for the finish thicknesses.
- Shelf life of the finish is 1 year from date of manufacture and shall be packaged in moisture sensitive packaging per IPC-1602

**5.10.7 HAL (Lead Free) RoHS**

- For lead free HASL the tin content shall be greater than 99%.
- SN100CL (Nihon Superior) lead free HASL specifically. Notify Benchmark if a different trademark finish is being utilized.
- Solder coating shall be 1.27 to 25.4 um (50 to 1000 micro-inches) thick.
- Composition is nominally 99.3% Sn, 0.6% Cu, and 0.1% other inhibitors and proprietary components. Copper is to be maintained between 0.60% and 0.85%.
- Solder thickness is to be measured where applicable by XRF at the geometric center of the pads. If there is a visibly thick area of the deposit, the thickness shall be measured at the thickest part of the solder. Pads selected for measurement must include: pads of the finest pitch (one pad in both the X and Y direction must be measured), pads of the next finest pitch, 50 mil pitch pads, and a capacitor/resistor pad. Measurements must be taken on both sides of the board. Isolated areas may be as low as 50 micro-inches if they maintain a solderable surface. The pad must be visually bright and smooth when viewed at 3X.
- XRF results shall be reported in Certificate of Compliance under Section 13 Supplier Deliverables.
- Shelf life of the finish is 1 year from date of manufacture and shall be packaged in moisture sensitive packaging per IPC-1602



### 5.10.8 Gold Contact Plating

Should the board require **selective, hard gold** plating for edge fingers, switch contacts, etc. an electrolytic plating process shall be used.

- Electroplate gold onto contact features per IPC-6012 Table 3-3, Code G. Class 2 minimum gold thickness is 0.8  $\mu\text{m}$  (31.5  $\mu\text{in}$ ). Class 3 minimum gold thickness is 1.25  $\mu\text{m}$  (49.2  $\mu\text{in}$ ). The minimum electroplated nickel thickness is 2.5  $\mu\text{m}$  (98  $\mu\text{in}$ ) per IPC-6012 Table 3-3, Code N.
- Nickel and gold plating shall be restricted to the contact areas. There shall be no extraneous, loose, or nodular Ni or Au plating on traces or adjacent plated holes.
- Electroplated gold shall have a smooth/shiny surface and it shall have no surface nodules from things like inclusions or a spongiform electroplating morphology.
- XRF results shall be reported in Certificate of Compliance per Section 13 Supplier Deliverables. Shelf life of the finish is 1 year from date of manufacture and shall be packaged in moisture sensitive packaging per IPC-1602.

### 5.10.9 Electroplated Nickel-Gold or Bi-Level Gold

Plate **contact features only** as mentioned in section 5.10.8. All the remaining, exposed features must be protected by one of the two following options to deliver thinner gold, reducing the opportunity for gold embrittlement of solder joints.

**Electroplate Ni(Flash)** 0.127 - 0.457 microns (5-18 micro-inches) Au on remaining exposed metal surfaces (solder pads) and soldered barrels ,or

**Electroless Gold** thickness shall adhere to **ENIG** finish requirements per IPC-4552 and measured using XRF.

- The nickel-gold electroplating process must not leave any of the underlying copper layer exposed.
- XRF results shall be reported in Certificate of Compliance per Section 13 Supplier Deliverables.
- Shelf life of the finish is 1 year from date of manufacture and shall be packaged in moisture sensitive packaging per IPC-1602.

### 5.11 Legend Marking and Board Identification

- Marking inks (silkscreen) used to apply legend must be indelible, non-nutrient, and nonconductive polymer inks. Color white unless otherwise specified.
- The cured legend ink must be opaque, readable, and permanent.
- There shall be no silkscreen ink on any metal surface like: SMT, component, or test point pad. The supplier is allowed to remove the offending areas on the legend artwork when necessary. The silkscreen is compliant to IPC-4781 type 2.
- Each printed board shall be marked with legend and/or etched markings that are legible in the area as specified on the fabrication drawing or in an open area of the printed board, so that they are visible after assembly. Any marking that is etched in copper must be

kept clear of etched circuitry. Such marking must maintain at least the minimum designed conductor spacing from the nearest conductor.

- A four-digit date code with permanent mark identifying the week and year (WWYY) of manufacture in the location shown on the printed board drawing, or open area. Date of manufacture shall be the actual week that the printed board is marked.
- Supplier may add additional markings to indicate manufacturing lot specific information with the condition such markings shall not interfere, obscure or affect any other required features.
- Printed boards conforming to the requirements of this Specification shall be UL Recognized Component, with flammability rating of 94V-0. Each printed board shall be marked with the supplier's Recognized Marking and Type Designation (per UL 796) and the UL flammability rating (94V-0) in the location shown on the printed board drawing, or open area near other markings.
- Unless otherwise defined in the fabrication drawing, the supplier's UL-registered logo and flammability rating must be etched in copper.
- Flex and rigid-flex boards are exempt from the UL 94V-0 approval status with the following requirements: All base materials and other materials, defined in the stack-up of the printed board design package shall be UL 94V-0 approved materials. The supplier must provide certification that declares all materials used are UL 94V-0 approved.

## 6 Electrical Test

- Unless otherwise specified, all boards shall be tested to IPC-9252, Table 4-1 for designated IPC Class.
- The supplier shall perform a net list comparison prior to test fixture development. Any discrepancies must be reported to BEI in writing for review.
- All boards shall pass an electrical net list test. Complete 100% test coverage is required, which includes all nets, test points, test point vias, and all pads not covered with solder mask. If net list data is not provided, or is in an unusable format, a net list is to be extracted from the supplied design package. However, if net list testing is a specified requirement on any customer specification, or part specific master drawing, BEI must be notified to determine if net list extraction is acceptable.
- Test programs shall not be made from a "golden board". Each board that passes electrical test shall be immediately stamped with each stamp using permanent non-conductive ink. Preferred placement of stamp is on the bottom side of the board near the supplier logo and date code. The stamp shall be visible after assembly, and shall not be on any solderable surface, test pad, or fiducial. The stamp is to be on the board, not the panel rails, if possible. If stamping is not possible the supplier shall notify Benchmark and receive written approval to deviate from this specification. Deviations will be on an individual part basis.

## 7 Hi-Pot Test

- HI-POT test, when required, will be specified on the fabrication drawing.

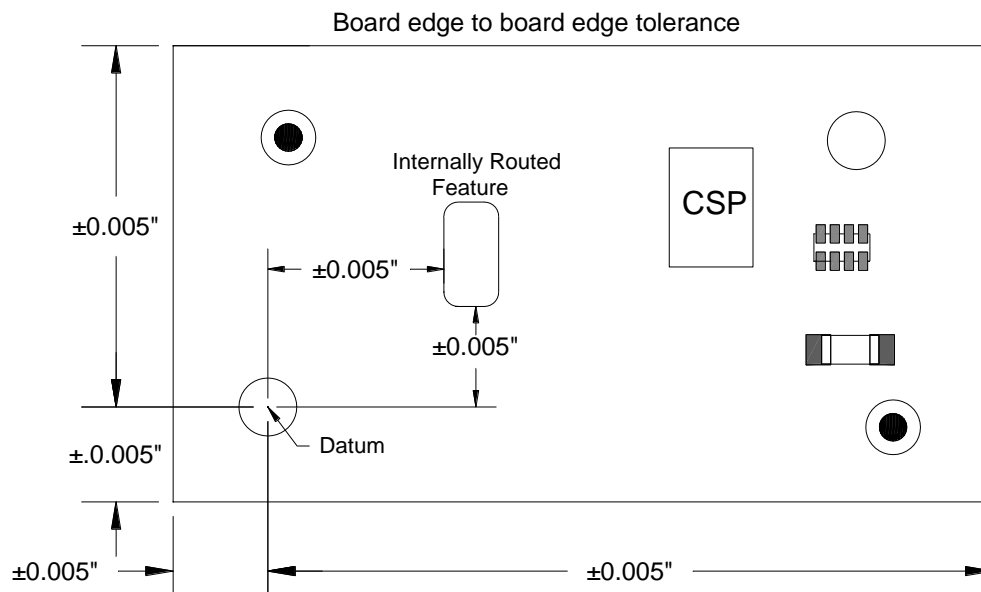
- For production 100% testing is expected.
- All tested printed boards shall be marked with a HP (HI-POT) stamp.
- Any board failing the hi-pot test shall be rejected as scrap and should not be retested.

## 8 Process Capabilities

When tolerances are not specified, the following apply:

Linear Tolerances .XXX =  $\pm 0.005$ "  
.XX =  $\pm 0.01$ "

Routed board edge to edge tolerance will be  $\pm 0.010$ ". Overall dimensional tolerance is  $\pm 0.005$ " from drilled datum hole to any external profiled (routed) board edge. Internal routed features shall have a tolerance of  $\pm 0.005$ " across the feature edges. See Figure 8-1.



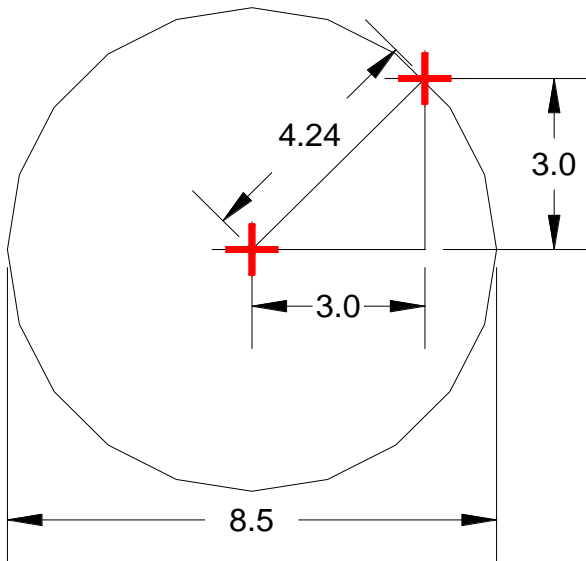
**Figure 8-1: Datum to Drill or Edge Feature**

Scored board edge to edge tolerance will be  $\pm 0.010$ ". Overall dimensional tolerance is  $\pm 0.005$ " from drilled datum hole to the center of the V-score.

Hole diameters specified for plated holes are to be considered as after plating and any surface finish.

- Non-plated tooling hole diameter tolerance is  $\pm 0.002$ ".
- Finished plated hole diameter tolerance is  $\pm 0.003$ ".
- Via holes with a finished diameter of 0.020" or less do not have a minimum hole size requirement, so tolerance is +0.003"/-100%. See **Filled and Capped Vias** for via treatment options.
- Press-fit finished hole size diameter tolerance is  $\pm 0.002$ ". Several press-fit design standards also dictate drill sizes.

- Holes > 0.220" may be nibble drilled or routed and have a  $\pm 0.005$ " tolerance.
- Non-plated and plated slots within the board outline have  $\pm 0.005$ " tolerance.
- Hole positioning shall be located within 0.0085" Diameter True Position for all hole locations ( $\pm 0.00424$ " positional tolerance). See Figure 8-2.

**Figure 8-2: DTP Hole to Hole**

The Radius True Position is defined as the square root of (delta X squared + delta Y squared).

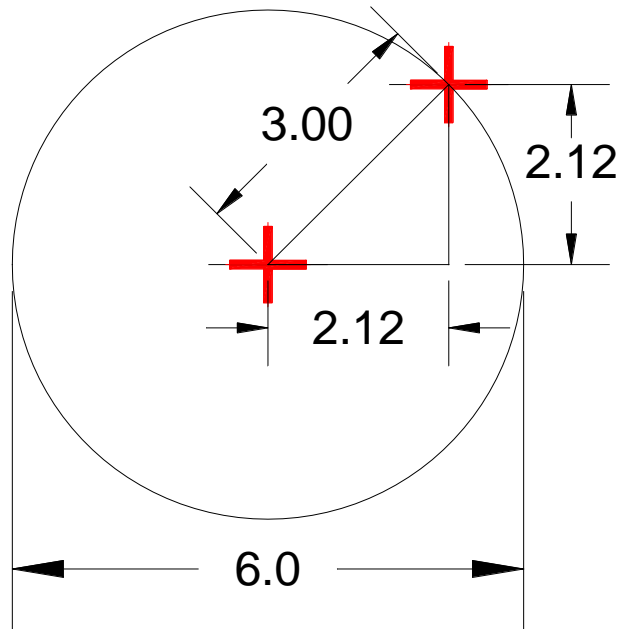
$$DTP = 2 * RTP$$

**Example:**

Let's say the center of the hole is located 3 mils right (X) and 3 mils up (Y) from the intended location. So  $\sqrt{(3)^2 + (3)^2} = \sqrt{18} = 4.24$  mils = Radius True Position, so the Diameter True Position would be  $8.48 \approx 8.5$  mils. The center of the hole must be located within this circle.

Copper feature to copper feature positioning:

- Features spanning < 12" shall be located within 0.006" Diameter True Position ( $\pm 0.003$ " positional tolerance) of the electronically defined coordinates (database or Gerber). See Figure 8-3.



**Figure 8-3: DTP Copper Features**

- Features spanning > 12" shall be located within 0.0085" Diameter True Position ( $\pm 0.00424$ " positional tolerance) of the electronically defined coordinates (database or Gerber).

## 9 Repairs

- There shall be no repairs to the plated through holes, annular rings, or traces specified as controlled impedance.
- Inner layer welds shall not exceed 1 per board per layer when performed prior to lamination. Inner layer repairs, after lamination, are unacceptable.
- The maximum length of a repaired trace is 1 inch (2.54 cm) long.
- Unless otherwise specified, there shall be a maximum of 1 open circuit repair performed to the external conductors on any board. No more than 10% of any lot may be repaired for open circuits. Repair per IPC-7721. The repaired area is to be covered with solder mask or epoxy.
- Boards with open circuits due to barrel voids, or any other plated-through-hole defect, shall be destroyed.

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## 10 Inspection

- All Benchmark products will have AOI inspection performed on all internal signal layers and a minimum of 10% of the power and ground layers in a production work order.
- All Benchmark products will receive 100% final visual inspection. The minimum magnification shall be a 3X halo light. The first piece from each lot shall be inspected using 10X magnification.

## 11 Micro-sectioning

- Cross-section samples shall include the smallest via hole, plated copper filled microvias (blind and buried) when present, and at least one component hole.
- Cross-sections must be taken such that interconnects in each layer are represented.
- Micro-section coupons from the border of the panels will be accepted if they have been proven to be representative of the conditions of the actual finished board.

## 12 Waiver Requests

- For any requested deviations the printed board supplier shall document the issue and include a proposed resolution. The waiver request should also state whether the job has been put on hold for resolution.
- Note: The job can continue to run for any deviations that affect the back end of the process only.
- Waiver requests shall be emailed to the SCA or purchasing agent listed on the Purchase Order. The standard Benchmark email address is <firstname.lastname@bench.com> however there are exceptions.
- The printed board supplier may request a product waiver for issues that are routinely flagged. Once a product waiver is approved by Benchmark, the printed board supplier is not required to seek Benchmark approval for any future builds of that same part number revision.

## 13 Supplier Deliverables

A Certificate of Compliance (C of C) shall be provided with each shipment. The C of C must include:

- Supplier name and division (manufacturing site)
- Benchmark part number and revision
- Date codes / Lot numbers including quantity of each
- List of lot serialization series or individual serial numbers (as applicable)
- Signature of authorizing person with Date
- Purchase order number
- A statement of RoHS compliance (Material Declaration for RoHS boards)

- 
- Laminate manufacturer and manufacturer part number (suppliers shall be able to show traceability to laminate lot codes)
  - Each new revision of a printed board shall be accompanied by two solder samples. These samples should represent the entire surface features and finish as defined on the fabrication and/or panelization drawing (mechanically good / may be electrically bad sample). A solder sample shall be provided with each batch lot shipped.
  - This sample shall be clearly identified, contained in a separate minimum protective package, and included in the shipping container. The container with the solder sample should be clearly marked and labeled as containing “solder sample.” The solder sample printed board must be clearly marked on both sides in a permanent fashion in a contrasting color by marker or label.
  - A First Article Inspection Report of all drawing dimensions and print requirements for first delivery of any new part number or revision is required. The supplier shall provide a copy of the report which must include:
    - Actual dimensional data
    - Tolerances
    - Pass or fail statement
    - Copy of print with associated reference points to the first article report, i.e., measurement 1, measurement 2 = M1, M2 (bubble drawing).
  - Controlled impedance reports where applicable per date code.
  - Cleanliness testing shall be performed in accordance with IPC-TM-650 Section 2.3.25.
  - The bath temperature of 80 degrees C shall be used. Using an alternate or ambient temperature of 22 degrees C would not be acceptable for our Certificate of Compliance.
  - The ionic contamination must meet or be below 1.00 ug/cm<sup>2</sup> (6.45 ug/inch<sup>2</sup>) of NaCl equivalents when tested with an Omegameter. Certificate of test, that includes test readings, shall be included with each shipment.
  - Where applicable a micro-section analysis (IPC-TM-650 Section 2.1.1 or 2.1.1.2 Micro-sectioning) report detailing the findings of the micro-section for each new date code along with the sections are required to be included with the shipment. This report shall include:
    - Photo of micro-section
    - Average and minimum copper plating thickness
    - Dielectric thickness (where required)
    - Overall plating quality and integrity
  - X-Ray Fluorescence (XRF) report prepared based on data taken in section 5.10 (Surface Finishes) shall be provided for all non-OSP alternative surface finishes including: ENIG, ENEPIG, Silver, Tin, HASL, SN100CL, flash gold and contact gold surface features.
  - An electrical test certification for every date code with the following information:
    - Quantity tested
    - Quantity accepted

- First pass yield percentage
- When the deliverables listed above cannot be met the supplier shall contact Benchmark to request a waiver. If approved, all waivers will be valid for only the issuing Benchmark site.
- Supplier deliverables will be maintained by Incoming Inspection and will have the same retention time as the inspection history.

## 14 Handling and Shipping Requirements

### 14.1 Moisture sensitivity

- The fabricator must follow moisture sensitivity guidelines per IPC-1602 for handling all lead-free capable laminates including:
  - Storage of material
  - Handling of material during processing
  - Baking material after each wet process regardless of processing method
  - Packaging of materials
- Benchmark may audit our fabricators to ensure moisture sensitivity procedures are in place and followed. Printed board fabricators must be able to demonstrate that their material suppliers adhere to J-STD-20 and J-STD-33 for material storage, handling, processing and shipping.
- Printed boards shall be packaged in moisture barrier bags that meet IPC-1602.
- The Water Vapor Transmission Rate (WVTR) for dry packaging of printed boards should meet the requirements of IPC-1602, which specifies a WVTR of  $< 0.002 \text{ gm/100 inch}^2$ . Moisture Barrier Bags (MBB) with lower WVTR values may be considered, to increase shelf life of the printed board package and reduce desiccant loading requirements.
- The bag should be heat sealed so as not to damage or cause delamination of the MBB. Full air evacuation is not recommended; light air evacuation will reduce the packaging bulk and enhance carton packing. Excessive evacuation may impede desiccant performance and lead to MBB punctures.
- Moisture barrier bags shall contain an amount of desiccant as defined by IPC-1602 (Appendix B) as a function of the MBB size and include a humidity indicator card. The desiccant pack(s) should be placed along the edges of printed boards inside the MBB. Desiccant material shall be dustless, non-corrosive, and sulfur free. The desiccant pack(s) and HIC should not make direct contact to the printed boards.



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## 14.2 Packaging

- Printed boards shall be packaged to prevent damage and surface scratching.
- The supplier shall maintain a documented Foreign Object Debris (FOD) Elimination Program.
- The supplier's minimum protective package shall assure no loss of solderability to meet expected shelf life based on board finish.
- 1 year shelf life: ENIG, ENEPIG, Flash Gold, Immersion Silver, SN100CL (LF HASL), and PB HASL
- 6 month shelf life: OSP and Immersion Tin
- Product stored at fabricator facility beyond shelf life listed herein shall be retested for and pass solderability requirements per IPC-6012 prior to shipment.
- If special storage (other than the environment listed previously) or preconditioning (pre-bake at a certain temperature, humidity level and time) is required to maintain solderability and prevent delamination, measling, discoloration, etc., it must be clearly stated on associated paperwork supplied with the shipped product.
- Unless noted otherwise in the notes, supplier may use their standard preferred packaging.
- Immersion Silver finished printed boards shall be covered with protective sulfur-absorbing paper (e.g., Silver Saver® paper) inside the MBB. Any separation sheets placed between boards shall be sulfur free (see 1.4.9) and pH neutral, or sulfur absorbing paper (treated on both sides). See IPC-4553 for additional information.
- Only boards of the same date or lot code may be sealed in the same bundle. Each MBB shall be labeled with part number, date/lot code and the quantity enclosed. The date or lot codes of all the boards contained in each box shall be printed on the outside of that box.
- All shipping containers shall be clearly labeled with printed board part number, date code or lot number, PO number, and quantity. Any shipping carton containing the C of C, solder sample, or X-outs, should be clearly labeled to identify enclosed items.
- All packing materials shall be non-static generating (the box to ship the order is exempt from this requirement). Packing "peanuts" of any type, shall not be used.
- Shipping container shall not exceed 40 lbs. (18.2 kg).

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### Revision History

Date	Rev	Reason for Change:	ECO Number:
02/14/2023	B	Updated document title to replace Printed Circuit Board with Printed Board to match change in IPC terminology. Entire document reformatted to latest template format. Updates to all sections with particular focus on solder mask and via treatments. Sections added for flex.	CORP005052